Application No.: 09/750,465   Docket No.: JCLA6707

In The Claims:

1. (Currently Amended) An apparatus for executing block data transfer instruction inside a processor after receiving decode information containing N bits, the apparatus comprising:

an adder for receiving the N-bit decode information and adding the N bits together to produce an initial count value;

a counter <u>connecting to the adder</u> for receiving the initial count value, decreasing the value by one after outputting a count control signal;

a register identification number generator that generates a plurality of register identification numbers equal in number to the initial count value according to the count control signal, wherein the register identification number corresponds to the bit positions in the N-bit decode information having a bit value '1';

a memory unit for holding data; and

a register list that includes a plurality of registers, wherein the register list is able to receive the register identification numbers so that stored data can be freely exchanged between the memory unit and the registers that correspond to the register identification numbers.

2. (Original) The apparatus of claim 1, wherein the apparatus further includes an address calculator for generating an address signal according to the decode information and then outputting the address signal to the memory unit so that data can be freely exchanged between the registers that correspond to the register identification numbers and the addressed memory in the memory unit according to the address signal.

3. (Original) The apparatus of claim 1, wherein the register identification number generator further includes N logic units for generating register identification numbers equal in number to the initial count value such that when the counter decrements by one down to zero, the N logic unit is able to generate corresponding register identification number according to the bit position in the N-bit decode information that has a value '1'.

4. (Currently Amended) A method of executing block data transfer instruction inside a processor after receiving an N-bit decode information, comprising the steps of:

adding the N bits together to form an initial count value;

receiving the initial count value and generating a plurality of register identification number identical in number to the initial count value, wherein the register identification number corresponds to the bit position of the N-bit decode information that has a bit value '1'; and

mapping linking up the a plurality of registers that correspond to the register identification numbers to and the a memory unit according to the register identification numbers so that stored data can be exchanged between the memory unit and the registers.

5. (Original) The method of claim 4, wherein the step for generating the register identification numbers includes the sub-steps of:

performing a count down operation decreasing the initial value count by one until the value zero is reached; and

generating a register identification number whenever a bit value of '1' is found in the N-bit decode information after each count down operation.

Application No.: 09/750,465   Docket No.: JCLA6707

6. (Original) The method of claim 4, wherein the method further includes generating an address signal according to the decode information so that stored data in the register corresponding to the register identification number and data within the memory unit having an address corresponding to the address signal can exchange with each other.

7. (NEW) A method of executing block data transfer instruction inside a processor after receiving an N-bit decode information, comprising the steps of:

adding the N bits together to form an initial count value;

outputting the initial count value as a count value;

determining if the count value has decrement to zero; and

if the count value is zero, the processing is completed, otherwise if the count value is non-zero, performs following checking steps:

sequentially check the N-bit decode information for a bit value of '1';

if a bit value of '1' is found, an identification number of one of a plurality of register is set to facilitate access;

setting the found bit whose bit value is '1' to '0';

decreasing the count value by one; and

repeating the checking steps until the count value is decreased to zero.

Page 5 of 11